

DIGI-LOG™ REVERB MODULE (BTDR-3)

A great digital reverb sound that easily replaces a spring reverberation unit

NEW ITEM



Pat. No. : US 8,204,240
CN ZL200880021110.9

Features

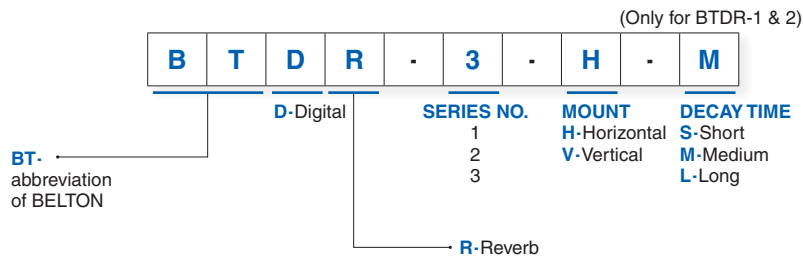
- Reverb depth (decay) adjustable via 2 external resistors or 1 dual pot
- Stereo outputs may be summed for mono operation
- Simple interface: input, output, +5V, and ground
- AC-coupled input and outputs require no external capacitor

Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Current	I_{CC}		60	100	mA
Input Voltage	V_{IN}			1.5	V_{PEAK}
Voltage Gain			-3		dB(each output)
Residual Noise			-77	TBD	dBV
Input Impedance	Z_{IN}		10k		Ω
Output Impedance	Z_{OUT}		220		Ω
Operating Temperature		-40		+85	C

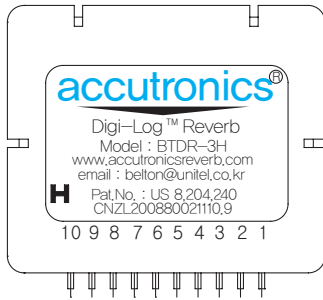
Subject to change without notice

Ordering code



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Connection Diagram

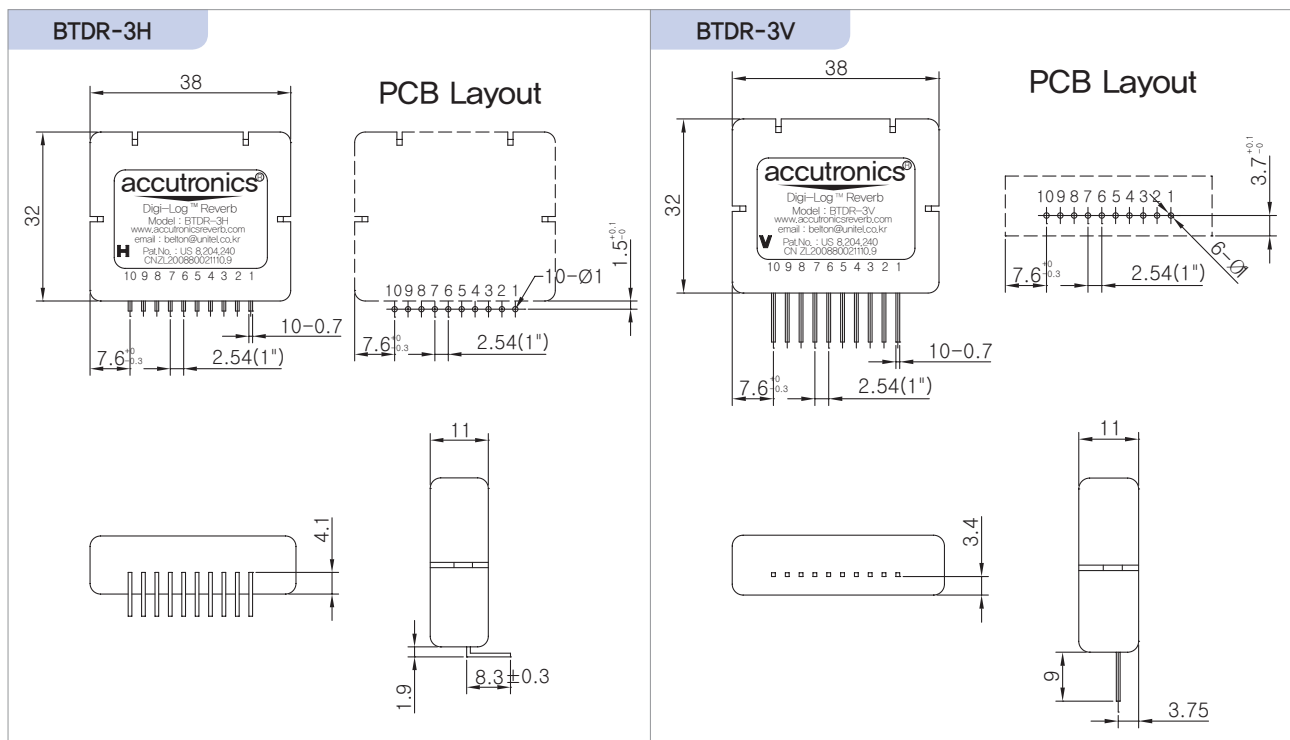


- | | |
|---------------|-------------|
| 1. +5V | 6. Output 1 |
| 2. Power GND | 7. Pot 1A |
| 3. Input | 8. Pot 1B |
| 4. Signal GND | 9. Pot 2A |
| 5. Output 2 | 10. Pot 2B |

Note : Pins 2 and 4 are internally connected.

See the Application Circuit for more information on how to connect the grounds.

Dimensions



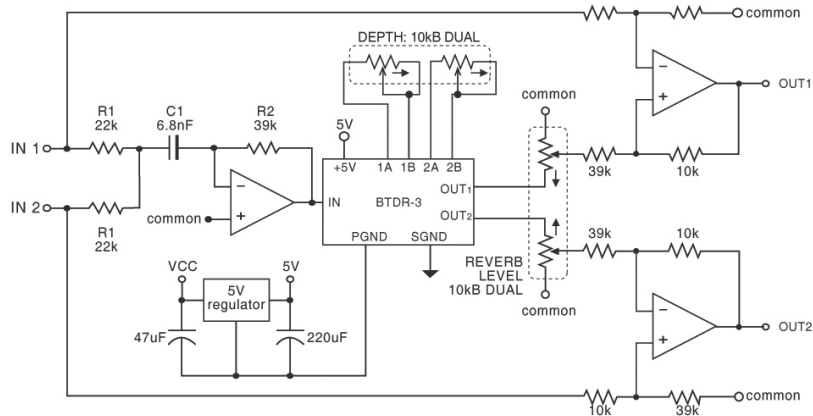
Applications

A regulated 5V supply is mandatory. An LDO regulator is recommended for battery-powered devices .

- The following example circuits are for instrument-level signals:
 - “Common” is “Signal GND” in a split-supply circuit or Vcc/2 in a single-supply circuit.
 - Audio noise during power-down can be minimized by quickly discharging supply from 5V to 0V; otherwise, external output muting may be necessary.
 - R1, R2 and C1 create a pre-EQ high-pass filter and may be adjusted to taste.
- The BTDR-3 was designed to work specifically with a 10k with a 10k pot, and consistent operation is not guaranteed with larger value.

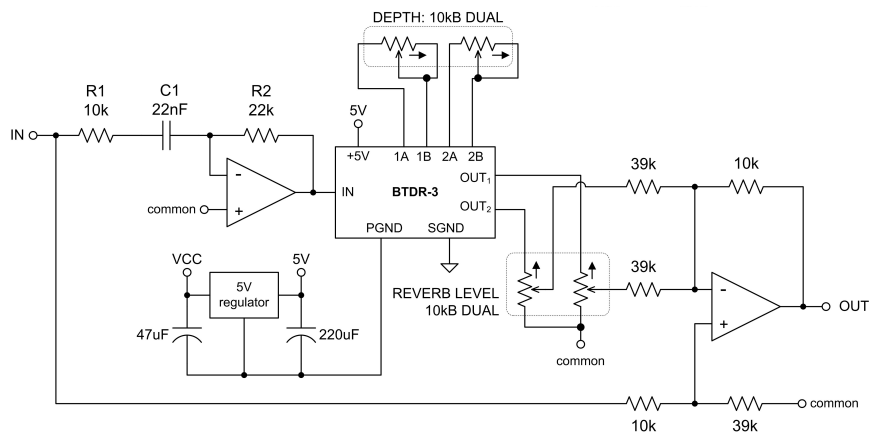
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Stereo Circuit



- High-pass frequency (Hz) = $1/(\pi \cdot C1 \cdot R1)$
- High frequency gain (dB) = $20 \cdot \log(2 \cdot R2/R1)$

Mono Circuit



- High-pass frequency (Hz) = $1/(2\pi \cdot C1 \cdot R1)$
- High frequency gain (dB) = $20 \cdot \log(R2/R1)$

Considerations for FCC Compliance

- The maximum internal clock frequency is approximately 14MHz .
- Although Accu-Bell believes that circuits employing solely the BTDR-2 will easily pass FCC Part 15, no guarantees of compliance are made; the circuit must be tested as a whole for radiated and conducted emissions.