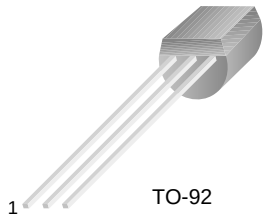
FAIRCHILD SEMICONDUCTOR®

December 2011

PF5102
N-Channel Switch

Features

- This device is designed for low level analog switching, sample and hold circuits and chopper stabilized amplifiers.
- Sourced from process 51.
- See J111 for characteristics.



TO-92

1. Drain 2. Source 3. Gate

Absolute Maximum Ratings* T_a = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	40	V
V_{GS}	Gate-Source Voltage	-40	V
I_{GF}	Forward Gate Current	50	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

1. These ratings are based on a maximum junction temperature of 150 degrees C.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics T_a = 25°C unless otherwise noted

Symbol	Parameter	Max.	Units
P_D	Total Device Dissipation Derate above 25°C	625 5.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	°C/W

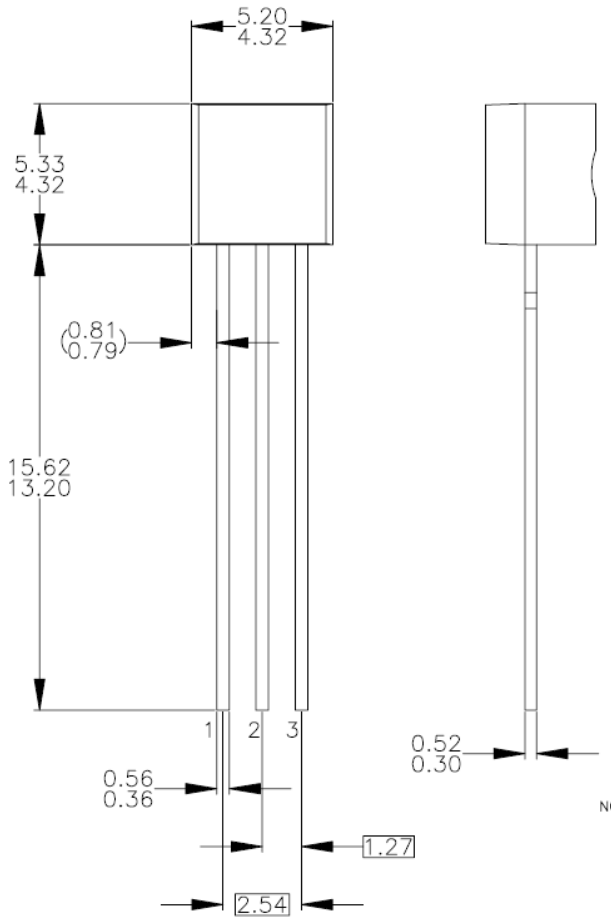
Electrical Characteristics T_a = 25°C unless otherwise noted

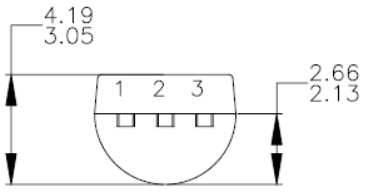
Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = -1.0μA, V_{DS} = 0	-40		V
I_{GSS}	Gate Reverse Current	V_{GS} = -15V, V_{DS} = 0 V_{GS} = -15V, V_{DS} = 0, T_A = 125°C		-1.0 -0.2	nA μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15V, I_D = 1.0nA	-0.7	-1.6	V
$V_{GS(f)}$	Gate-Source Forward Voltage	I_G = 1.0mA, V_{DS} = 0		1.0	V
On Characteristics					
I_{DSS}	Zero-Gate Voltage Drain Current *	V_{DS} = 15V, V_{GS} = 0	4.0	20	mA
Small Signal Characteristics					
g_{fs}	Forward Transfer Conductance	V_{DS} = 15V, V_{GS} = 0, f = 1.0KHz	11,000		μmhous
g_{oss}	Output Conductance	V_{DS} = 15V, I_D = 500μA, f = 1.0KHz		25	μmhous
C_{iss}	Input Capacitance	V_{DG} = 15V, V_{GS} = 0, f = 1.0MHz		16	pF
C_{rss}	Reverse Transfer Capacitance	V_{DG} = 15V, V_{GS} = 0, f = 1.0MHz		6	pF

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.0%

Physical Dimension

TO-92





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Dimensions in Millimeters