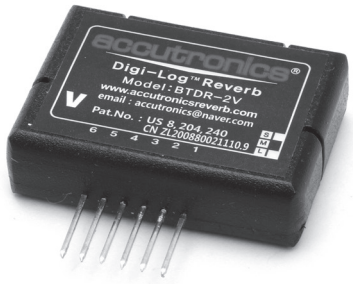
DIGI-LOG™ REVERB MODULE (BTDR-2)

BELTON

A great digital reverb sound that easily replaces a spring reverberation unit



Pat. No. : US 8,204,240
CN ZL200880021110.9

Features

- Small package is half the size of the BTDR-1
- Stereo outputs may be summed for mono operation
- Simple interface requires only input, output, +5V, and ground
- AC-coupled input and outputs require no external capacitors

Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Current	I_{CC}		60	100	mA
Input Voltage	V_{IN}			1.5	V_{PEAK}
Voltage Gain			-3		dB(each output)
Residual Noise			-77	TBD	dBV
Input Impedance	Z_{IN}		10k		Ω
Output Impedance	Z_{OUT}		220		Ω
Operating Temperature		-40		+85	C

Preliminary, Subject to change without notice

Available Options

	Decay		
	S	M	L
Type	short	medium	long
Time(T_{60})	2.0 s	2.5 s	2.85 s

Ordering code

(Only for BTDR-1 & 2)

B	T	D	R	-	2	-	H	-	M

- **BT-** abbreviation of BELTON
- **D**-Digital
- **R**-Reverb
- **SERIES NO.** 1, 2, 3
- **MOUNT** **H**-Horizontal, **V**-Vertical
- **DECAY TIME** **S**-Short, **M**-Medium, **L**-Long

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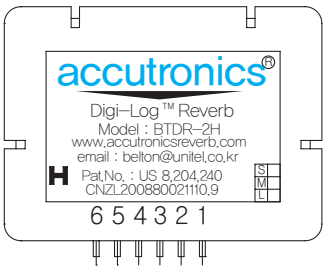
Connection Diagram

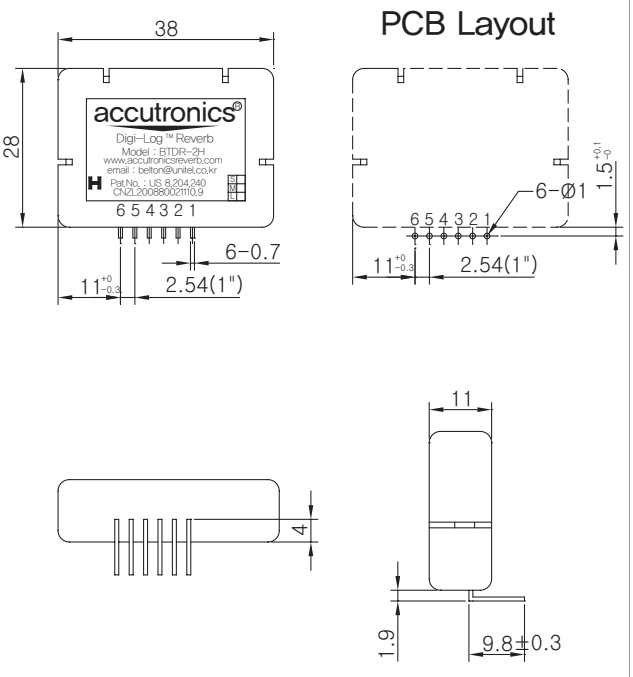


1. +5V
2. Power GND
3. Input
4. Signal GND
5. Output 2
6. Output 1

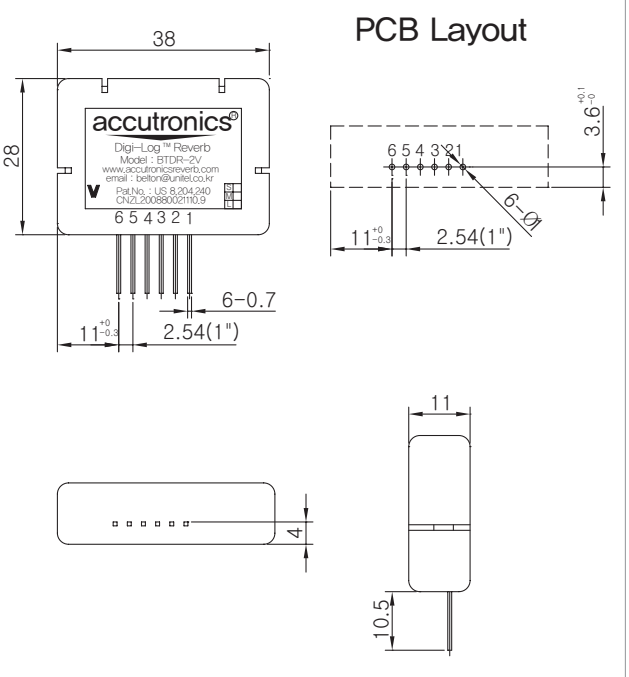
Note Pin 2 and 4 are internally connected. See the Application Circuit for more information on how to connect the grounds.

Dimensions

BTDR-2H



BTDR-2V



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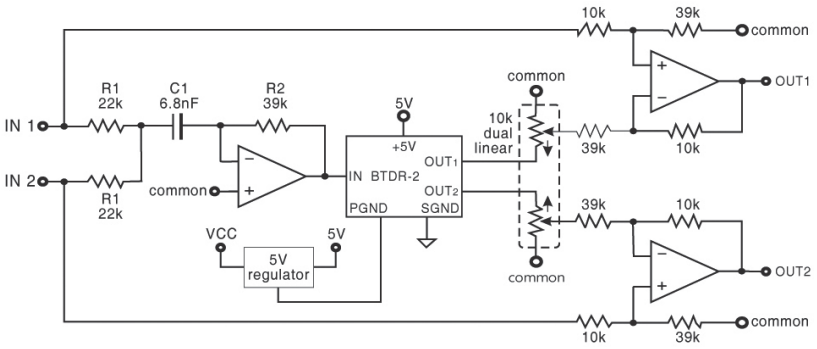
Application Circuit

A regulated 5V supply is mandatory. An LDO regulator is recommended for battery-powered devices.

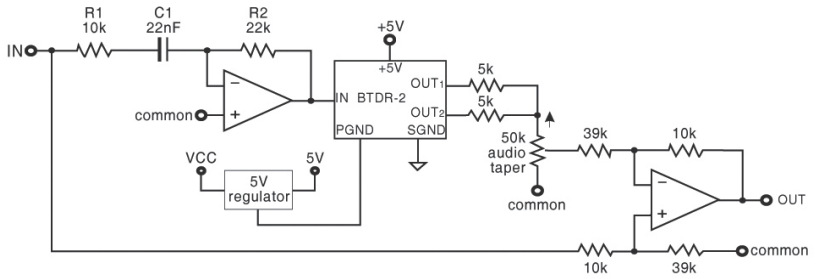
- The following example circuits are for instrument-level signals :
  - "Common" is "Signal GND" in a split-supply circuit or $V_{cc}/2$ in a single-supply circuit.
  - Audio noise during power-down can be minimized by quickly discharging supply from 5V to 0V; otherwise, external output muting may be necessary.
  - R1, R2 and C1 create a pre-EQ high-pass filter and may be adjusted to taste.

Stereo Circuit



- High-pass frequency (Hz) = 1/(π • C1 • R1)
- High frequency gain (dB) = 20 • log(2 • R2/R1)

Mono Circuit



- High-pass frequency (Hz) = 1/(2π • C1 • R1)
- High frequency gain (dB) = 20 • log(R2/R1)

Considerations for FCC Compliance

- The maximum internal clock frequency is approximately 14MHz.
- Although Accu-Bell believes that circuits employing solely the BTDR-2 will easily pass FCC Part 15, no guarantees of compliance are made; the circuit must be tested as a whole for radiated and conducted emissions.